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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/664,585	09/17/2003	Hiroshi Masuya	81751.0066	3682

26021 7590 10/17/2005

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/664,585	MASUYA, HIROSHI	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *August 11, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7,9-11 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7,9-11 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on August 11, 2005 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5-7, 10-11 and 21are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto (US 6169323) in view of Masaki (US 6166446).

Regarding claim 1, Fig. 4 of Sakamoto shows a semiconductor device comprising:

a die pad [a portion marked in slashes beneath the chip 2];

a semiconductor chip [2] and bonded to the die pad;

an inner lead [an inner portion of the lead 4] having a sloping section sloping upward and outward when a surface of the die pad which semiconductor chip is bonded faces upward;

a wire [3] electrically connecting the inner lead to semiconductor chip;

a sealing section [1] sealing the inner lead, the semiconductor chip, and the wire;

and

an outer lead [a portion labeled 4a] extending outward from the sealing section.

Fig. 4 of Sakamoto shows substantially the entire claimed structure except an electrode on the semiconductor chip and the wire connection to the electrode. Masaki disclose an electrode on the on the semiconductor chip (col. 4, lines 16-18) on which the wiring is connected.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Masaki into the device of Sakamoto in order to have the electrodes on the semiconductor chip to accommodate the design specification.

Regarding claim 5, Fig. 1 of Masaki shows the inner lead [101] further has a second sloping section sloping downward and outward from a higher end of the sloping section.

Regarding claim 6, Fig. 1 of Masaki shows the inner lead further has a portion extending in a horizontal direction and connected to the outer lead.

Regarding claim 7, the combined teachings of Fig. 4 of Sakamoto and Fig. 1 of Masaki shows a bonding position between the wire and the inner lead is lower than the position of the electrode.

Regarding claim 10, Fig. 8 of Sakamoto shows a circuit board [5] on which the semiconductor device is mounted.

Regarding claim 11, Sakamoto discloses an electronic instrument comprising the semiconductor device [col. 1, lines 58-63].

Regarding claim 21, Fig. 4 of Sakamoto shows a semiconductor device comprising:

an inner lead [an inner portion of the lead 4] having a sloping section sloping upward and outward, when a surface of the die pad which the semiconductor is bonded faces upward;

a die pad [a portion marked in slashes beneath the chip 2];

a semiconductor chip [2] and bonded to the die pad;

a wire [3] electrically connecting the inner lead to the semiconductor chip;

a sealing section [1] sealing the inner lead, the semiconductor chip, and the wire; and

an outer lead [a portion labeled 4a] extending outward from the sealing section.

Fig. 4 of Sakamoto shows substantially the entire claimed structure except "the inner lead further has a second sloping section sloping downward and outward from a higher end of the sloping section" and an electrode on the semiconductor chip and the wire connection to the electrode. Masaki disclose an electrode on the on the semiconductor chip (col. 4, lines 16-18) on which the wiring is connected.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Masaki into the device of Sakamoto in order to have the electrodes on the semiconductor chip to accommodate the design specification. In addition, Fig. 1 of Masaki shows the inner lead [101] having a second sloping section sloping downward and outward from a higher end of the sloping section. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Masaki into the device of Sakamoto in order to have the inner lead with a second sloping section sloping downward and outward from a higher end of the sloping section to evenly distribute the weight exerted by the chip.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto and Masaki as applied to claim 1 above, and further in view of Glenn (US 6143981).

Regarding claim 9, the combined teachings of Sakamoto and Masaki show the most aspect of the instant invention except "a surface of the die pad opposite to the semiconductor chip is exposed from the sealing section." Fig. 9 of Glenn shows a surface of the die pad opposite to the semiconductor chip is exposed from the sealing section.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Glenn into the device of Sakamoto and Masaki in order to have a surface of the die pad opposite to the semiconductor chip exposed from the sealing section to reduce the package size.

Response to Arguments

Applicant's arguments filed July 14, 2005 have been fully considered but they are not persuasive. The rejection stands and new rejections are made in response to Applicant amended claims. In addition, the examiner presents the remarks below in response to Applicant's arguments.

Applicant mainly argues that "In particular, the applied references do not disclose or suggest, "an inner lead having a sloping section sloping upward and outward, when a surface of the die pad which the semiconductor chip is bonded faces upward." As discussed above, the combined teachings of Sakamoto and Masaki show that an inner lead having a sloping section

sloping upward and outward. And both of Sakamoto and Masaki show that a surface of the die pad which the semiconductor chip is bonded faces upward.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

Steven Loke